Remarks

Applicants thank the Examiner for the careful examination of this application and the clear explanation of the rejections.

The amended title conforms to the claimed invention.

The amended specification updates reference to a related patent and prior patent applications from which priority is claimed.

The new claims "particularly point out and distinctly claim the subject matter the applicant regards as his invention."

Claim 3 finds support at paragraph [0056] of the published specification.

Claim 3 defines a process of selecting TAP connections in an integrated circuit having plural cores with each core having a TAP. Each TAP is coupled to a TLM, which selects one of the TAPs. The TAPs and TLM operate in accordance with the IEEE 1149.1 test interface.

The process performs an IEEE 1149.1 instruction scan operation with a TAP instruction augmented with a TLM scan code.

The process performs an IEEE 1149.1 data scan operation with TAP selection data to load the TLM with new TAP selection information.

The process performs IEEE 1149.1 instruction and data scan operations on the TAP selected with the new TAP selection information.

In contrast, US 5,689,516 to Mack discloses:

> A programmable logic device (PLD) includes test circuitry compatible with the JTAG standard (IEEE Standard 1149.1). The PLD also includes a programmable JTAG-disable bit that can be selectively programmed to disable the JTAG circuitry, leaving the PLD to operate as a conventional, non-JTAG-compatible PLD. The PLD also includes means for testing the JTAG test circuitry to determine whether the JTAG circuitry is defective, and means for programming the JTAG-disable bit to disable the JTAG circuitry if the testing means determines that the JTAG circuitry is defective. [Abstract]

The patent to Mack fails to teach or suggest the limitations of claim 3 of performing an IEEE 1149.1 instruction scan operation with a TAP instruction augmented with a TLM scan code; performing an IEEE 1149.1 data scan operation with TAP selection data to load the TLM with new TAP selection information; and performing IEEE 1149.1 instruction and data scan operations on the TAP selected with the new TAP selection information.

Claim 3 stands allowable.

Claims 4-7 also stand allowable as depending from allowable independent claim 3 and as including additional distinguishing limitations.

Claim 4 requires scanning the TLM scan code through an instruction register of a TAP and then into the TLM.

Claim 5 requires scanning the TLM scan code through an instruction register of a TAP and then into an augmentation instruction shift register in the TLM.

Claim 6 requires maintaining IEEE 1149.1 instruction and data scan operations on the TAP selected with the new TAP selection information.

Claim 7 requires performing an instruction register update, disabling scan access to the currently selected TAP, and enabling the performing an IEEE 1149.1 data scan operation with TAP selection data to load the TLM with new TAP selection information

Providing a programmable JTAG-disable bit that can be selectively programmed to disable the JTAG circuitry, as disclosed in the patent to Mack, fails to teach or suggest the limitations of the depending claims.

The application is in allowable form and the claims distinguish over the cited references. Applicants respectfully request reconsideration or further examination of this application.

Respectfully Submitted,

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